COLLABORATION PROPOSAL

FOR THE IMPLEMENTATION OF FAST ARITHMETIC UNITS

Join us in a revolution of the field of computer microprocessors and cloud computing, unlocking untapped mathematical potential that will redefine computing performance across multiple sectors including Machine Learning, AI and neural network training, Digital Signal Processing, cryptography, and many more. Together, we will be able to develop the next generation of processors, that are faster, more energy efficient and ready for the future, as well as new software-based mathematical encryption schemes to set new standards of privacy, reliability and efficiency in cloud computing.

My mathematical research provides an optimal representation of all mathematical objects and structures [1,2], with the potential to revolutionize computer science and applied mathematics. By leveraging this new mathematical description and developing practical applications, we seek to create value by offering efficient technological solutions to a range of industries. Applications include a general method for time and energy efficient Fully-Homomorphic Encryption (FHE), as well as a new processor architecture with unique capabilities and characteristics that can replace the existing Von-Neumann Architecture with a Computing-In-Memory scheme, which is key in achieving time and energy efficient AI and Neural Network training (market share study found on page 20). Through strategic partnerships and collaborations, we are poised to drive innovation and create a competitive edge in the rapidly evolving technological landscape, countering diminishing returns [3,4]. This document focuses on the Computing-In-Memory processor architecture. A separate proposal will discuss applications to Low-Level Languages, and energy and time efficient homomorphic encryption (often referred to as the Holy Grail of Cryptography).

REPORT AUTHOR

Juan P. Ramírez

ALLIANCES
Partners / Clients

We look to work with experts, institutions and businesses

DEVELOPMENT

By working with our clients, we are able to provide custom designed and tailor-fitted critical subunits for digital and analog devices.

Collaborations

Applications and Integration

TEAM

Sr. Engineers

Research
Math - Physics - CS

INDUSTRY

We are positioned to be a driving froce that will impact almost any sector of science and technology.

Revision of mathematical foundations with efficient operations and other applications.

LEADERSHIP

RESEARCH

Through strategic partnerships and collaborations, we will create a competitive edge.

Middle and Final Customer Satisfaction.

INNOVATION

VALUE

PRODUCTS AND SERVICES

First we focus on a new generation of simple yet powerful processors of unmatched capabilites.

A proposal of new mathematical methods yields results in applied physics, numerical methods, cryptography, data mining, high-performance computing among others.

Effective Campaigns

Globally competitive patents for digital and analog systems.

Mathematically optimized architectures for data science, cryptography, analog and digital devices.

MARKETING AND CUSTOMER EXPERIENCE

THEORETICAL FRAMEWORK

Through a fundamental solution to the problem of numerical representations and their computational complexity, we seek to transform the computing industry. This initiative is based on a major revision of mathematical foundations that allows fast and low-powered calculation of mathematical operations. The mathematical framework is given in the paper shown below [1]. This article and other supporting papers are cited in the bibliography, at the end of this proposal.

Canonical Set Theory with Applications from Parallel Matrix Operations and Data Structures to Homomorphic Encryption

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July 7, 2023

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Abstract

Few questions have resounded through the mind of the mathematician, as much as the simple question of describing the nature of a number. The longstanding consensus is that it does not matter which set theory is used to describe numbers. What matters is that it can be done. It is widely believed that the particular choice of a construction for natural and real numbers is irrelevant for the rest of mathematics. Here, a set theory is proposed as a canonical theory that yields transparent proofs in fundamental areas of mathematics including group theory, discrete mathematics, analysis, data types, and new results tying these areas and addressing Hilbert's 24-th (twenty-fourth) Problem and Benacerraf's Identification Problem. Applications to computer science include a model for Homomorphic Encryption, and a linearly-scaleable circuit that serves for parallel addition and multiplication of scalars, vectors and matrices, with wide implications for Area-Specific Integrated Circuits (ASICs) used in CGI, Neural Networks and AI training, Dimensionality Reduction for Machine Learning at Software and Hardware Level, Digital Signal Processing, among other applications that depend on fast and low-powered vector operations. This low-power In-Situ (In-Memory) computing architecture, based on a patent-pending Simple and Linear Fast Adder (SLFA), is a direct consequence of the proposed set theory. Algebraic invariants are also described with results bringing together set theory, discrete mathematics, number theory and algebraic structures. A canonical block form is defined for the Cayley table of finite groups, in terms of the numeric representation of groups. Automorphisms, and the minimal independent system of equations that define the group are given by the block form, among other information regarding groups' internal and external structure. The proposed construction of natural numbers is generalized to provide a simple and transparent construction of the continuum of real numbers, with a fast approximation for the numeric derivative that can be implemented with the SLFA. Infinite data structures are defined in the most efficient way with the smallest possible data type. A countable sequence of real numbers is coded in a single real number, and an infinite $\infty \times \infty$ real-valued matrix is also coded with a single real number. A real function is coded in a set of real numbers, and a countable sequence of real functions is also coded in a set of real numbers. These codings are meaningful and computable. Mathematical objects of all types are well assigned to tree structures in a proposed hierarchy of types.

Keywords: Structuralism; Set Theory; Fast Adder; Arithmetic Logic Unit; Finite Group; Real Number; Fast Derivative; Data Types; Tree; Complexity; Matrix Multiplication; Fully-Homomorphic Encryption

The single most important subunit determining performance, for almost any processor, is the ALU (Arithmetic Logic Unit) which is responsible for more than 60% of all the operations executed in an average CPU, and more than 80% of operations executed in an average GPU [5]. The ALU is even more important, for area-specific integrated circuits (ASIC) used in AI training, data centers, aviation [6], automobiles, communications, geolocation, crypto-mining [7], energy sector, advanced CGI applications, Digital Signal Processing among others. More reference material on ALUs and their functionality, architecture, and specifications are found in [8-13].

The most important subunit of an ALU is the Adder. The article above proposes new foundations of mathematics with applications essential to information technologies and computer sciences including a Simple and Linear Fast Adder (SLFA) with optimized efficiency, complexity, dimensions, and materials costs, that is pending Patent Cooperation Treaty (PCT) approval. A modified version of the SLFA is compatible with proposed fast-multiplication and fast-derivative (FDA) algorithms, and vector/matrix operations.

The FAU (Fast Arithmetic Unit) is a new type of ALU of its own kind with unparalleled performance and efficiency in computing everything from addition of scalars to matrix multiplication (essential for machine learning/AI and neural network training, CGI, Digital Signal Processing), in one simple and scaleable circuit.

Problem:

Von-Neumann Architecture is characterized for making two separate units, one for memory and one for arithmetic logic, and connecting them *via* a bus. This creates a bottle neck in computational throughput because data migration between memory and logic is very expensive and generates huge delay. The need for new architectures and fundamental changes to the approach in designing classic computational schemes has become more apparent in the last years.

Solution:

In-Memory Computing is a concept solution proposed decades ago, but still has fundamental challenges to be overcome before it can be fully implemented. The theoretical framework in [1] allows for the implementation of a simple circuit, here referred to as Fast Arithmetic Unit (FAU). It solves major issues for In-Memory Computing [14] and it is capable of executing low-powered In-Situ ALU operations faster and cheaper, improving overall processor efficiency, in an area smaller than the area occupied by a traditional fast-adder. This unit is also capable of calculating a fast-derivative approximation (FDA), and fast vector multiplication, making the FAU of central importance for AI hardware and other TPU (Tensor Processing Unit) applications that require processing vector/matrix operations faster and cheaper.

Why FAU?

Replacement of traditional ALUs for FAU technology, in general and specific use processors, will:

-Significantly Improve Performance
-Unparalleled Capabilities and Characteristics
-Optimized Energy Efficiency
-Compatibility with Many Industries
-Solution for In-Memory Computing
-One-size fits-all Circuit for all ALU Operations

What's Next?

1. Develop FAU prototypes that improve on efficiency and performance and integrate the FAU architecture to existing standards.

2. Collaborate with ASIC designing teams and adapt our technology to their needs, in order to secure contracts and financing of operations.

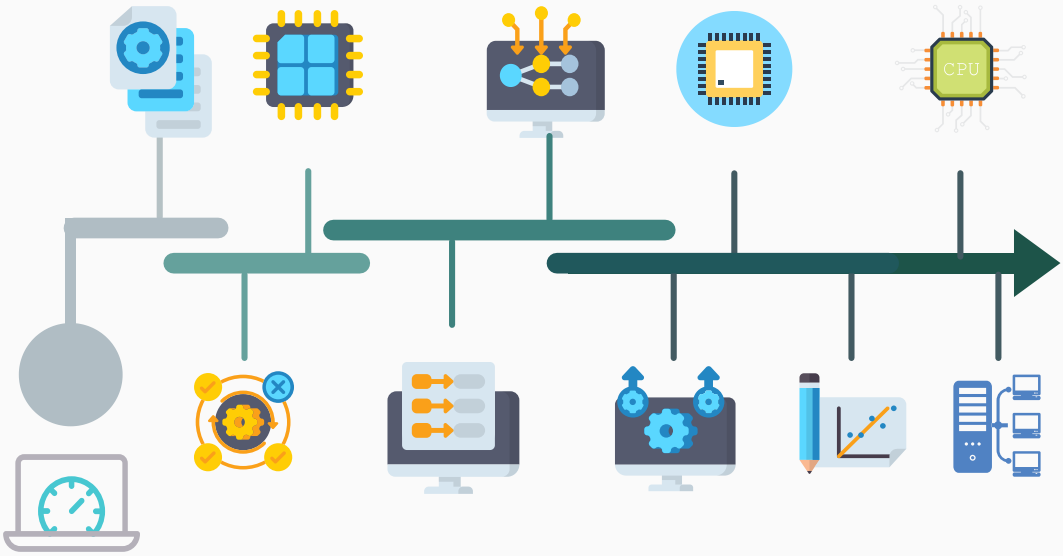
3. Facilitating the replacement of traditional ALUs with FAU, in ASICs.

4. Consolidating research and developing capabilities for integrating FAU to high-performance VLSI architectures.

PROGRESS STAGES

0. Validation
1. First R+D Stage: Identifying Immediate Industries, Patents, Prototypes
2. Integration to ASIC Design Standards
3. Integration to ASIC Production Standards
4. Second R+D Stage: Consolidating Research
5. Digital Operations and Output Management (GPU and CPU)

Progress:
We have succesfully started progress on stages 0 and 1 with an initial patent application on the SLFA.



STAGE (0): VALIDATION

Summary

In an area smaller than other fast adders, the FAU is able to execute fast addition and multiplication, and other operations such as subtraction and division, in terms of these. Furthermore, the FAU can fast approximate a numerical derivative (FDA), giving the FAU unmatched capabilities, functionality and efficiency, all in a simple design with minimum surface area.

The two main activities for this stage are 1) Simulating the proposed architecture for FAU and 2) Publishing and comparing results with existing ALU architectures [15,16].

Simulating

During this stage, simulations on the implementation of the FAU are carried out using tools such as VHDL, Verilog and FPGA.

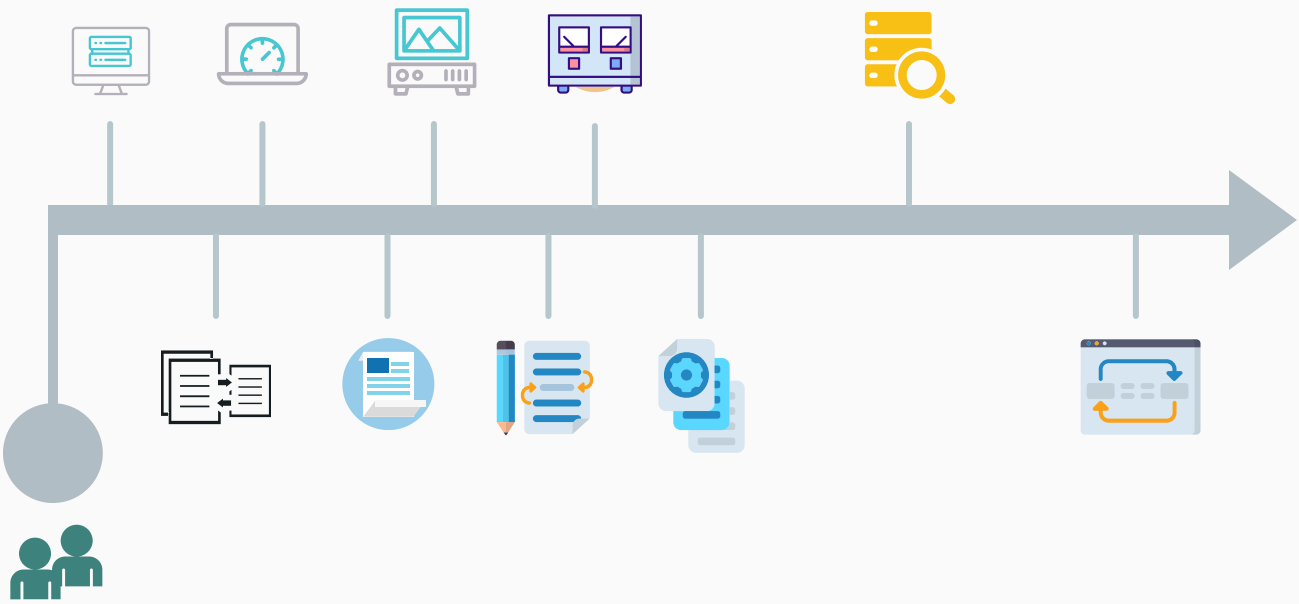
Publishing

The simulation results are compared and evaluated against results from existing architectures.

The conclusions are to be shared in international editorials and will help determine resources, objectives and strategies for the next stages.

OBJECTIVES FOR STAGE (0)

- Build a Core R&D Team
- Simulate Fast Arithmetic Unit (FAU) Architecture
- Publish Results
- Conclusions and Planning for Next Stages



THE TEAM FOR STAGE (0)

A team of specialists in Computer Science, physics and mathematics will lay the groundwork for specialized, state-of-the-art, arithmetic units to be implemented in high-performance processors.

The team will be able to propose and expand new lines of research for Computing-In-Memory architectures, control units for ASICs, material optimization, operation optimization, non-classic architectures such as photonic computing schemes, cryptography, AI and Neural Network training HW.

Hardware

A team of C.S. Engs. with experience in ALU architecture to determine best materials, configurations, instructions, layouts, i/o to CU and other variables through FPGA simulations.

Software

The initial simulations need to be carried out in collaboration with a team of SW Engs. using FPGA and HW description languages (HDL) such as Verilog and VHDL.

Mathematics

A team of mathematicians covering the basic areas of number theory, mathematical analysis, matrix analysis, computational geometry, AI, Probability Theory, Finite Mathematics and Combinatorics, Algebra and Logics, will help to choose the best research topics for later stages.

Physics

An important part of the initial research is dependent of a physics team to complement the research with the Electromagnetic Theory, Signal Processing, Material Science for Semiconductors, among others topics.

STAGE (1): IDENTIFYING IMMEDIATE INDUSTRIES, PATENTS, PROTOTYPES

Summary

ALUs are circuits implemented on different scales, for different applications, with different materials, configurations, layouts and topologies, distinct kinds of memory elements, etc. This makes the FAU a disruptive technology applicable to a wide variety of industries.

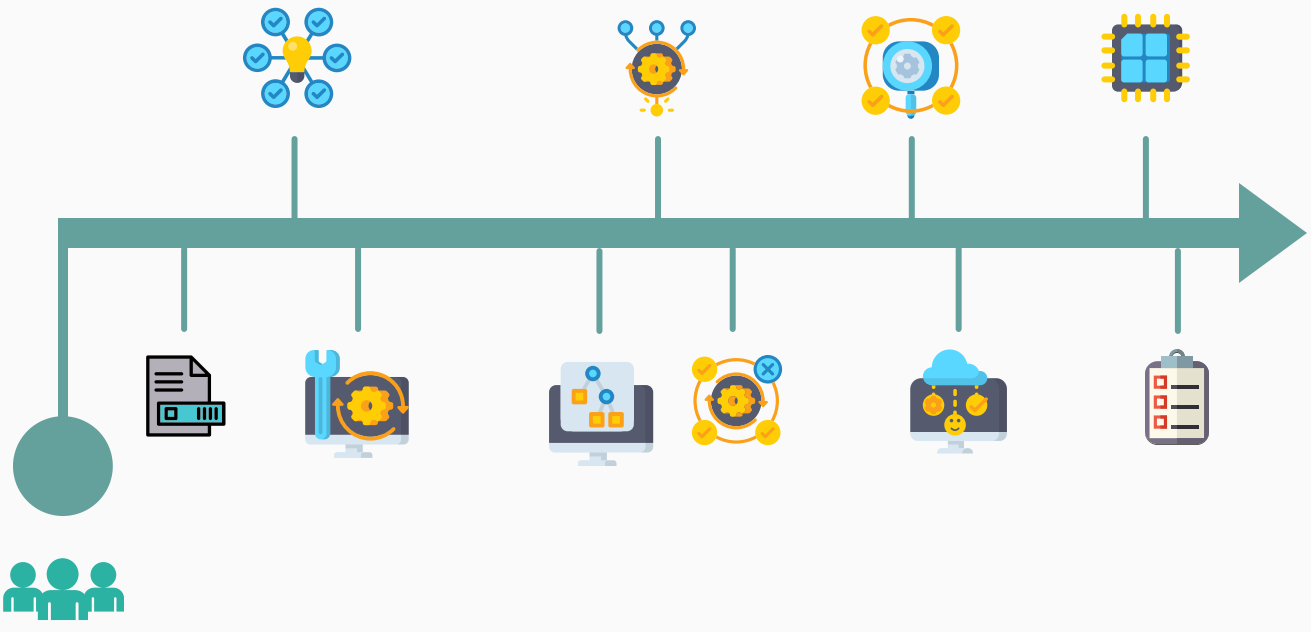
This stage comes after a careful evaluation of the main applications. In this stage we will look for the best industries for immediate implementation by identifying the simplest processors that can benefit most from the FAU in a fast and seamless manner.

Immediate implementation candidates are selected by taking into account technical analysis, company objectives, and market demand. Then, we secure the respective patents and designs that are prioritized for immediate implementation.

The main objectives of this stage are to design, evaluate and improve prototypes for the selected industries.

OBJECTIVES FOR STAGE (1)

- Consolidate and Expand the Team
- Identify Critical Patents from the Theoretical Framework
- Reduce Candidate Implementations Prioritizing Quickness and Simplicity
- Identifying Industries and Clients for Immediate Implementation
- Developing and Evaluating Prototypes



THE TEAM FOR STAGE (1)

Meeting the goals set out for this stage will require the expansion of our core team in Architecture and Hardware to include a technical base in design and prototyping of ASICs, centered on the In-Situ computing scheme of the SLFA whcih is pending PCT patent approval).

The SW team will need expertise in Low-Level Languages (LLL) for conducting research on the appropriate LLL that will help to integrate the FAU into existing assembly.

ALU Architecture

The HW team will need to include specialists on ALUs and Registers/memory elements.

Integrated Circuits

Operations in the HW area will require a knowledge base in designing and prototyping stages of ICs.

Software

For Assembly Language we will require the participation of SW specialists on LLL, Computational Logic and Information Theory.

STAGE (2): INTEGRATION TO ASIC DESIGN STANDARDS

Summary

Once the immediate implementation industries are recognized and prioritized by simplicity and speed of integration, along with their preliminary technical aspects, we proceed to integrate the FAU to current design standards.

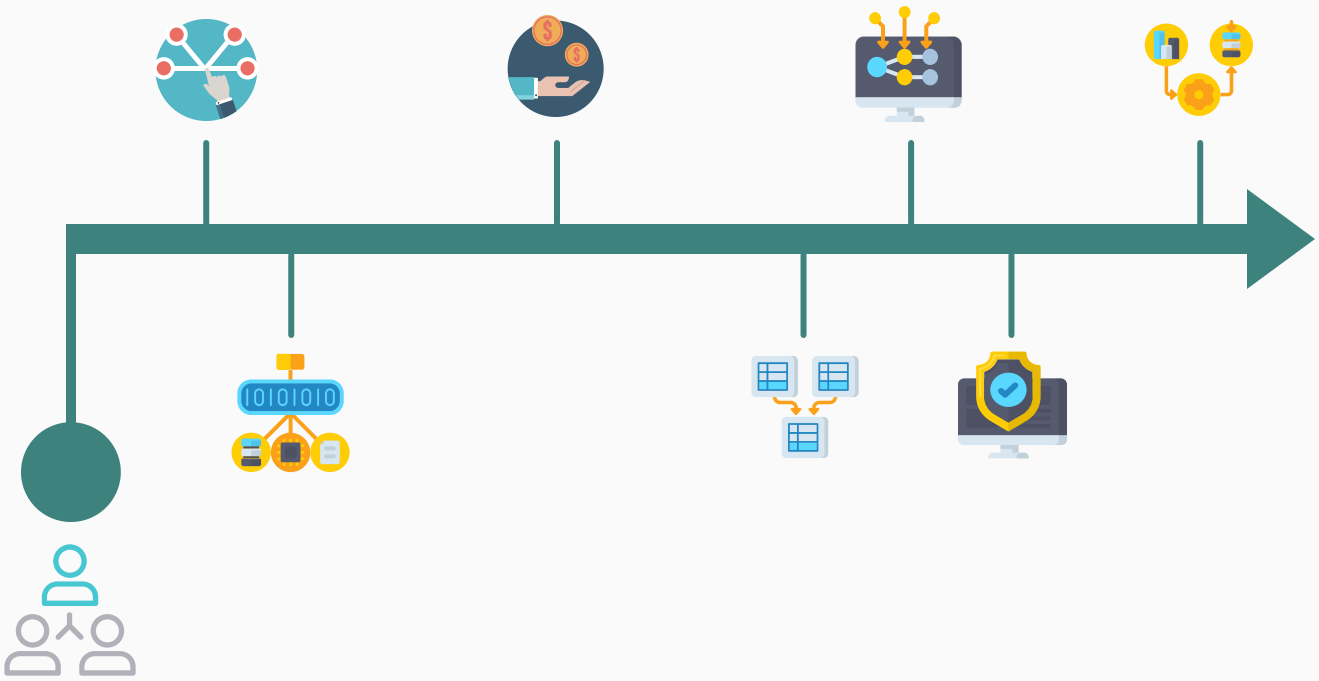
We seek collaboration with participants in the processor industry to replace existing ALUs with FAU architecture. The first applications will be in medium scale integration circuits with simple Control Unit. These can include commercial use ASICs used in smart appliances and electronics, GPS, automobiles, energy sector, communications, mathematical research, data mining, etc.

During this stage we look to collaborate, by contract, with ASIC manufacturers from different commercial and scientific applications, in order to secure continuity of operations.

Our potential clients and partners for this stage are mostly in Singapore, India, S. Korea, Russia, China, Japan, Germany, France, UK, and US. Strategic collaborations could include names such as Singapore Semiconductor Industries Association; Tata Elxsi, Vedanta; Hana Micron, Samsung Electronics; Sitronics, Mikron Group; SMIC, Pythium, Foxconn, HiSilicon; Japan Advanced Semiconductor Manufacturing, Fujitsu; Infineon Technologies AG, Siemens; STMicroelectronics; Arm; Texas Instruments, Qualcomm, Amkor, Xilinx, Altera, ONSEMI, Analog Devices Inc., Intel, etc.

OBJECTIVES FOR STAGE (2)

- Find Sr. Engs. and Team Leadership
- Establish Collaboration with Industry Clients
- Secure Contracts for Integrating FAU in ASICs
- Integrate Our Designs to Client Standards
- Simplify the Replacement of Traditional ALUs for FAU



THE TEAM OF STAGE (2)

The incorporation of FAU into ASICs requires collaboration with clients. In this stage new variables are considered such as i/o to CU for parametrizing "Clock", instruction sets, connections, etc.

Control Unit (CU)

We must work with clients' teams in charge of CU architecture for ASICs.

Registers

In particular, we must work with teams in charge of memory registers.

Software

Collaboration with our clients' LLL teams responsible for machine and assembly language.

Hardware

Other HW aspects outside the CU such as connections, buses, i/o control, etc.

STAGE (3): INTEGRATION TO ASIC PRODUCTION STANDARDS

Summary

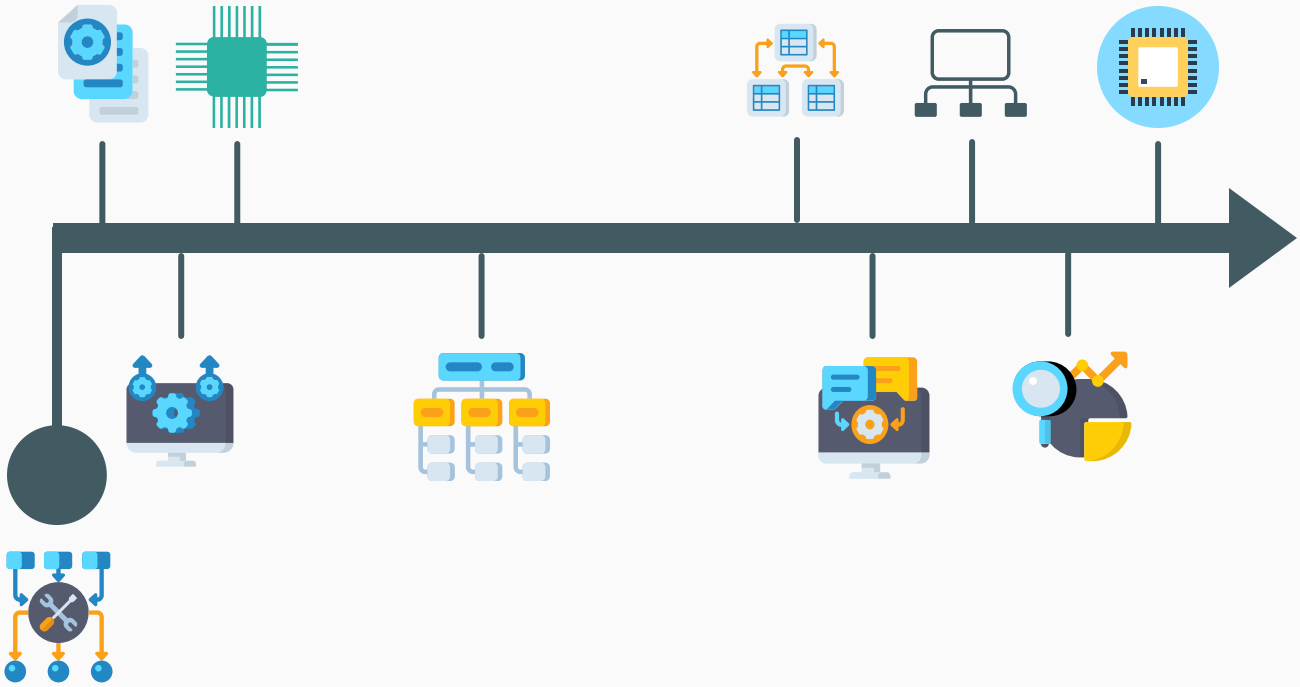
In the previous stage, we work together with our clients' teams during the designing stages of their ASICs, substituting the ALU for an FAU tailored to their specific needs.

The objectives of this new stage are divided in two. First, that our clients conclude successful production of processors with FAU technology. We maintain collaboration during their transition to production, as they may require it. Cooperation with them will be essential during testing, troubleshooting, quality monitoring, etc.

Secondly, this stage will serve to develop our internal capabilities. Among them, the implementation of the FAU to a larger class of ASIC architectures.

OBJECTIVES OF STAGE (3)

- Helping Our Clients Conclude Successful Production of ASICs with FAU Technology
- R+D for implementing FAU in Additional Platforms
- Achieving Universality of FAU in ASICs

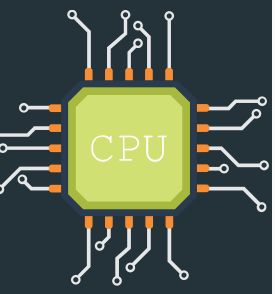


STAGE (4): CONSOLIDATING RESEARCH

Summary

Developing necessary capabilities for a complete implementation of designing stages of VLSI circuits. We wish to implement FAU into more profitable architectures such as general purpose RISC and other high-performance architectures with broad functionality.

During this stage, we drive R+D into other areas and applications proposed in the theoretical framework. These include topics in Numerical Methods, Matrix Analysis, Cryptography, Applied Physics, Finite Mathematics, Algebra, Data Science, and more.



STAGE (5): DIGITAL OPERATIONS AND OUTPUT MANAGEMENT

Summary

The previous stage has the purpose of developing basic capabilities in design and integration of FAU into VLSI architecture. During this stage we develop a production model for high-performance general and specific purpose architectures. This serves to continue our growth projections in market share, and to satisfy a growing demand on integrating computational efficiency, in all of its stages and levels from HW to SW.

MARKET SHARE PROJECTIONS

FAU technology can significantly improve microprocessor efficiency and performance and can be applied in a wide range of industries including consumer electronics, data centers, finance, AI systems, transportation, research and many others.

Let us take AI, as an example. In a study, by MarketsandMarkets, this industry is estimated to grow from USD $28 billion in 2020 to USD $126 billion by 2025, representing a compound annual growth rate (CAGR) of 34.5%. It is estimated that by 2030, the total market value will be USD $807 billion.

According to another report, by Precedence Research, the global AI microprocessors market is projected to grow from USD $16.86 billion in 2022 to USD $227.48 billion in 2032, representing a CAGR of 29.72%. Participation in only a fraction of the AI microprocessors market represents great revenue opportunities.

The long-term trend of microprocessors market share in the AI industry will be between 20% and 30% of total industry capitalization. A participation of just 1% with 20% profit margin means more than USD $80 million in potential net income, for the year 2026 alone.

In 2021 the total capitalization value of automobile CPUs was estimated at USD $53 billion. And these are just a few examples. FAU technology has the potential for competitive innovation in many sectors of science and technology.

Applications of the FAU can be adapted and scaled to other industries and applications from those mentioned, creating more revenue sources. By focusing on the long-term potential of this technology and developing a strategic plan for commercialization and growth, we can achieve a high ROI for our investors.

To secure the necessary resources for research and development, we seek strategic collaborations and partnership with ASIC manufacturers from all over the world, as well as building a strong brand and reputation of innovation and quality. As our ally, you will be greatly benefited by this unique focus into microprocessors and other critical technologies and acquire a strategic advantage in the changing technological landscape.

Join us in this exciting journey and let's make history together. Thank you!

Juan P. Ramírez
Project Leader

STRATEGIES

Leadership

- New approach to state-of-the-art designs for critical subunits in special and general-purpose architectures.
- Exploring new research areas with applications to high-performance computing.

Innovation

- Driving the development of optimized subunits.
- Collaboration in R+D, with partners of relevant industries and institutions.
- Innovate industrial and academic research by reformulating applicable mathematical foundations.

Services and Products

- Integrating mathematically optimized designs into digital and analog systems.
- High-value utility patents with global competitivity in digital and analog devices.

Marketing and Customer Experience

- Web Development.
- Effective Campaigns.
- Middle and final customer satisfaction.

EARLY TACTICS

- Validate new ALU architectures and compare the results to existing designs.
- Generate world class Research in Applied Mathematics and Computer Sciences.
- Participation in key international conferences and symposiums.
- Collaboration and strategic alliances with clients and partners.
- Early marketing strategies for connecting to general and targeted public.

MISSION

Maintaining our clients at the forefront of fundamental
processes in digital technologies
through global high-value patents and world-class R+D.

As well as the responsible integration of technological solutions
and the exploration of state-of-the-art applications that enrich experiences for
general public, scientists and artists.

VISION

Modern anthropological sciences and technological development from AI
to Social Organization, are product of interactions between
humanities and natural sciences.

The greatest challenges that science must solve are related to human realities and
are growing in complexity and breadth.

Recognizing that the nature of our most critical problems is socio-technical,
a better comprehension of solutions and implementations will be possible.

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Guadalajara, Jalisco, México

EDUCATION

UNIVERSIDAD DE GUADALAJARA

2008 - 2011, Guadalajara, México

- Teaching experience
- Served in panels for designing new academic programs in Natural Sciences and Engineering
- Participation in research and industrial application programs
- Speaker at Conferences and Seminars
- Developing and solving mathematical models for Theoretical Physics, with Dr. Georgi Pogosyan of the International Center for Advanced Studies and the Joint Institute for Nuclear Research
- Applied Mathematics with Dr. Alexander Yakhnov, from the Dpt. of Mathematics
- Director of extra-curricular academic events such as workshops and the "Art and Science Week"

UNIVERSIDAD DE GUANAJUATO Y CENTRO DE INVESTIGACIÓN EN MATEMÁTICAS (CIMAT)

2011 - 2013, Cd. Guanajuato, México

- Research presented at area-specific conferences and seminars
- Experience in mid-level and low-level programming languages
- Activities divulging mathematical sciences

LANGUAGES

English
Spanish
C++
Python

RESEARCH AREAS

Mathematics

Physics

Computer Sciences

RESEARCH TOPICS

- General Theory of Systems
- Mathematical Analysis
- Axiomatic Basis and Mathematical Foundations
- Numeric Solutions
- Recursivity
- ALU Architecture
- Computability and Complexity
- Category Theory
- Logical Systems
- Formal Systems and Languages
- Cryptography and Homomorphic Encryption
- among other related topics.

PARTICIPATIONS

- Conference on Recursive Solutions for Constant Coefficient Differential Equations (U. de G. 2010)
- Conference on Axiomatic Basis for Probability (Second School on Logic and Sets, UNAM campus Morelia, 2013)
- Conference on General Theory of Systems and Algebraic Structures (Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2017)
- Conference on A Natural Construction of Real Numbers (Physical-Mathematical Sciences Week, Universidad de Guadalajara)
- Workshop on Mathematics and Paint (Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2018)
- Conference on Topologies of N, in the Construction of R (Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2018)
- Organization and Direction of Art and Science Week at Universidad de Guadalajara, including workshops, conferences, roundtables and creation of Mural Inteligente (2018).
- Workshop on Mathematics and Paint (Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2018)
- Workshop on Higher Order Derivatives for Solving Partial Fractions and their Applications (XIII Encuentro de Especialistas del Norte de Jalisco y Sur de Zacatecas, 2018).
- "The Nature of Numbers" (Logic and Foundations Special Session available online, 52 Mexican Congress of Mathematics, Monterrey, Nuevo León, 2019)
- "The Nature of Numbers" (Universidad de Guanajuato/CIMAT, 2019)
- Chicago Quantum Summit (University of Chicago, 2020)
- Mural Inteligente (Inauguration of 55 Mexican Congress of Mathematics, 2022)
- "Simple Representation of Natural and Real Numbers" (Logic and Foundations Sessions, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022)
- "Simple and Linear Fast Adder based on a Simple Representation of Natural and Real Numbers" (Computer Science Sessions, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022)
- "Canonical Block Form for Finite Groups" (Algebra, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022)
- "A Pseudo Measure on the Space of Finite Functions and Permutations" (Algebra, 56 Mexican Congress of Mathematics, San Luis Potosí, 2023)
- "An Algorithm for Fast Multiplication and Addition of Multiple Inputs and it's Implementation for In-Memory-Computing" (Computer Sciences, 56 Mexican Congress of Mathematics, San Luis Potosí, 2023)

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