Search History:

Limited Classification Search

The Patent Analyst performed a limited classification search within the following US, IPC, CPC, ECLA, or F-Term classification areas:

CPC Class/Subclass(es): G06F 7/575; G06F 7/42; G06F 7/5055; G06F 7/556; G06F 7/443; G06F 7/502; G06F 7/5045; G06F 7/505; G06F 7/5095; G06F 7/52; G06F 7/57; G06F 7/76 (2023.08)

IPC (8) Class/Subclass(es): G06F 7/575; G06F 7/505; G06F 7/556; G06F 7/42; G06F 7/5055; G06F 7/443; G06F 7/502; G06F 7/5045; G06F 7/5095; G06F 7/52; G06F 7/57; G06F 7/76 (2023.01)

U.S. Class/Subclass(es): 708/232; 708/277; 708/236; 708/210; 708/211; 708/212; 708/234; 708/252; 708/256; 708/306; 708/402; 708/490; 708/505; 708/512; 708/517; 708/524; 708/534; 708/705; 708/706; 708/707; 708/708; 708/710; 711/109; 711/137; 711/214

See Global Search Results.

Global Patent Literature Text Search

The Patent Analyst performed the following global text search, which was not limited by classification but may or may not have been limited by other criteria:

Questel Orbit: https://www.orbit.com

#	Search query	Results
1	("ONE BIT REGISTER" AND "FOUR BIT REGISTER")/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
2	("LINEAR FAST ADDER" AND ("ARITHMETIC LOGIC UNIT" OR ALU))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
3	("LINEAR FAST ADDER" AND ("ARITHMETIC LOGIC UNIT" OR ALU))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
4	("LINEAR FAST ADDER")/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
5	(("ARITHMETIC LOGIC UNIT"))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
6	((LINEAR 1W FAST 1W ADDER))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
7	(LINEAR 1W ADDER)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	651
8	((ARITHMETIC 1W LOGIC 1W UNIT))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	72200
9	((((LINEAR 2W ADDER) 2D FAST+))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/T	0

	X/DESX AND (((ARITHMETIC 1W LOGIC+ 1W UNIT) OR ALU))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX)	
10	((LINEAR 2W ADDER) AND ((ARITHMETIC 1W LOGIC+ 1W UNIT) OR ALU))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	16
11	((LINEAR 2W ADDER))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	861
12	((LINEAR 2W ADDER) 3D FAST+)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
13	((LINEAR 2W ADDER) 6D FAST+)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	1
14	((LINEAR 2D ADDER) 6D FAST+)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	1
15	((4 OR FOUR) 1W BIT 1W (ADDER OR REGISTER))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	3111
16	((FOUR OR ONE) 1W BIT 1W (ADDER OR REGISTER))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	6914
17	(("1" OR ONE) 1W BIT 1W (ADDER OR REGISTER))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	7737
18	16 AND 17	4259
19	16 10D 17	4145
20	(11 10D 16 10D 17 10D 8)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
21	((11 10D 16 10D 17)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX AND ((ARITHMETIC 1W LOGIC 1W UNIT) OR ALU)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX)	0
22	(11 10D 16 10D 17)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
23	18 AND ((ARITHMETIC 1W LOGIC+ 1W UNIT) OR ALU)	165
24	(((FOUR OR ONE) 1W BIT 1W (ADDER OR REGISTER)) 10D (GATE 1W DEPTH))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	0
25	((CONSTANT OR STEADY OR STABLE) 1W GATE 1W DEPTH)/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	5
26	(G06F-007/42 OR G06F-007/443 OR G06F-007/505 OR G06F-007/5055 OR G06F-007/52 OR G06F-007/5095 OR G06F-007/57 OR G06F-007/575)/CPC	2677

27	(G06F-007/42 OR G06F-007/443 OR G06F-007/505 OR G06F-007/5055 OR G06F-007/52 OR G06F-007/5095 OR G06F-007/57 OR G06F-007/575)/IPC	9638
28	19 AND 27	234
29	19 AND 26	84
30	19 AND 26	84
31	29 NOT 28	15
32	(708402000 OR 708210000 OR 708211000 OR 708212000 OR 708232000 OR 708234000 OR 708236000 OR 708252000 OR 708256000 OR 708277000 OR 708277000 OR 708306000 OR 708512000 OR 708490000 OR 708505000 OR 708517000 OR 708512000 OR 708524000 OR 708534000 OR 708705000 OR 708706000 OR 708707000 OR 708708000 OR 708710000 OR 711109000 OR 711137000 OR 711214000)/PCLM	2233
33	26 OR 27 OR 32	11889
34	7 AND 33	8
35	11 AND 33	16
36	19 AND 33	285
37	(26 OR 27) AND 32	367
38	((PLURAL+ OR MULTIPLE OR MANY OR SEVERAL OR ADDITIONAL) 4D (("1" OR ONE) 1W BIT 1W (REGISTER+)))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	292
39	((LINEAR 3W ADDER))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	1260
40	((LINEAR 3W FAST 3W ADDER+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	0
41	(((LINEAR 3W FAST 3W ADDER+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND (((ARITHMETIC 2W LOGIC+ 2W UNIT) OR ALU))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	0
42	(((LINEAR 3W ADDER))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND (((ARITHMETIC 2W LOGIC+ 2W UNIT) OR ALU))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	43
43	(((LINEAR 3W ADDER))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND (((4 OR FOUR) 1W BIT 1W (ADDER+)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	1
44	(((LINEAR 3W ADDER))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND ((("1" OR ONE) 1W BIT 1W (REGISTER+)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	7
45	((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D ("AND GATE") 20D (POWER ADJ1 DISSIPAT+)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	0

46	((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D ("AND GATE")) AND (POWER 1W DISSIPAT+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	0
47	((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D ("AND GATE")))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	0
48	((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D ("XOR GATE")))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	0
49	((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D (GATE)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	123
50	(((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D (GATE)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND (((POWER OR ENERGY OR VOLTAGE) 2W (DISSIPAT+ OR REDUC+ OR TAPER OR CHOKE)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	10
51	(((((("4" OR FOUR) 1W BIT 1W (ADDER+)) 20D (GATE)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND (((POWER OR ENERGY OR VOLTAGE) 3D (DISSIPAT+ OR REDUC+ OR TAPER OR CHOKE)))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	20
52	((LOGARITHMIC 1W DELAY))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	61
53	((LOGARITHMIC 2W DELAY))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	112
54	53 AND 33	3
55	53 AND 39	0
56	53 AND 38	0
57	16 OR 17	10392
58	53 AND 57	1
59	53 AND 8	3
60	53 AND 7	0
61	((LOGARITHMIC 3D DELAY))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX	461
62	53 AND 61	112
63	53 AND 59	3
64	61 AND 33	8
65	61 AND 39	1
66	61 AND 38	0
67	61 AND 57	9
68	61 AND 8	8
69	61 AND 7	0
70	(((CONSTANT 2W GATE 2W DEPTH))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND ((CONSTANT 2W POWER 2W DIISSIPAT+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	0

71	(((CONSTANT 2W GATE 2W DEPTH))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND ((POWER 2W DIISSIPAT+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	0
72	(((CONSTANT 2W GATE 2W DEPTH))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX AND ((POWER 2W DISSIPAT+))/TI/AB/CLMS/OBJ/ADB/ICLM/KEYW/TX/DESX)	0
73	((("4" OR FOUR) 2W BIT 2W (ADDER+)))/TI/AB/OBJ/ADB/ICLM	215
74	(("AND GATE"))/TI/AB/OBJ/ADB/ICLM	0
75	((("4" OR FOUR) 2W BIT 2W (ADDER+)))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	2455
76	(("AND" 1W GATE))/TI/AB/OBJ/ADB/ICLM	377695
77	(("16" OR SIXTEEN) 3D ("AND" 1W GATE))/TI/AB/OBJ/ADB/ICLM	4026
78	(("16" OR SIXTEEN) 2W ("AND" 1W GATE+))/TI/AB/OBJ/ADB/ICLM	1754
79	(("16" OR SIXTEEN) 2W ("AND" 1W GATE+))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	18656
80	75 10D 79	1
81	75 30D 79	2
82	75 AND 79	44
83	(("XOR" 1W GATE+))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	23282
84	(("4" OR FOUR) 2W ("XOR" 1W GATE+))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	874
85	79 AND 84	19
86	((CONSTANT 2W GATE 2W DEPTH))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	6
87	(((CONSTANT OR STEADY OR STABLE) 2W GATE 2W (DEPTH OR WIDTH OR HEIGHT OR CAPACITY OR FLOW)))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	273
88	(((CONSTANT OR STEADY OR STABLE) 2W (POWER OR ENERGY OR VOLTAGE OR ELECTRICITY OR ELECTRICAL) 2W (DISSIPAT+ OR USAGE OR LOAD OR REDUC+ OR FLOW)))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	23990
89	87 AND 88	1
90	75 AND 88	0
91	76 AND 88	566

92	76 10D 88	2
93	76 20D 88	3
94	75 AND 76	180
95	75 10D 76	2
96	75 30D 76	4
97	75 40D 76	7
98	75 60D 76	7
99	(("AND" 1W GATE))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	1243816
100	75 60D 99	71
101	(("4" OR FOUR) 3W (("XOR" OR (EXCLUSIVE 1W "OR") OR "EOR") 2W GATE+))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	2537
102	84 10D 79	1
103	101 10D 79	5
104	((("4" OR FOUR) 3W (INPUT OR BIT) 3W (ADDER+)))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	4481
105	104 10D 61	0
106	104 AND 61	6
107	(LOGARITHMIC 3D (DELAY OR PROPAGATION))/TI/AB/CLMS/DESC/ODES/OBJ/ADB/ICLM/KEYW/TX/DESX	793
108	104 10D 107	0
109	104 AND 107	6
110	(G06F-007/502 OR G06F-007/5045 OR G06F-007/556 OR G06F-007/76)/IPC	3510
111	(G06F-007/502 OR G06F-007/5045 OR G06F-007/556 OR G06F-007/76)/CPC	1247
112	110 OR 111	3728
113	107 AND 112	4
114	104 AND 112	51
115	87 AND 112	1
116	101 AND 112	12

Google Patents: https://patents.google.com

#	Search query	Results
1	(linear ADJ1 fast ADJ1 adder) AND ((Arithmetic ADJ1 Logic ADJ1 Unit) OR ALU)	81,868

2	((Arithmetic 1 ADJ1 Logic ADJ1 Unit) OR ALU) AND (linear ADJ1 fast ADJ1 adder)	49,878
3	((Arithmetic 1 ADJ1 Logic ADJ1 Unit) OR ALU) AND (linear ADJ1 fast ADJ1 adder) AND ((1 OR one) ADJ1 bit ADJ1 (register))	27,722
4	((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND ((4 OR four) ADJ1 bit ADJ1 (adder*))	27,563
5	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND ((4 OR four) ADJ1 bit ADJ1 (adder*)	5,564
6	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND" ADJ1 gate*))	4,120
7	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND gate"))	689
8	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND gate") NEAR20 (power ADJ1 dissipat*))	57
9	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("XOR gate") NEAR20 (power ADJ1 dissipat*))	19
10	inventor:(Juan Pablo Ramirez)	8
11	(linear ADJ2 fast ADJ2 adder*)	100,000+
12	("4" OR four) ADJ1 bit ADJ1 adder*	100,000+
13	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 fast ADJ2 adder*) WITH (logarithmic ADJ1 delay)	10,322
14	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 fast ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (dissipat* OR load OR reduc*))	9,330
15	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (low OR dissipat* OR load OR reduc*))	9,513
16	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (low OR dissipat* OR load OR reduc*)) WITH (constant ADJ1 gate ADJ1 depth)	2,856

17	((("4" OR four) ADJ1 bit ADJ1 adder*) WITH ((power OR voltage OR energy) ADJ2 (decreas* OR low OR dissipat* OR load OR reduc*)) WITH (constant ADJ1 gate ADJ1 depth) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR)) AND (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) AND (logarithmic ADJ1 delay)	2,856
18	((("4" OR four) ADJ1 bit ADJ1 adder*) 5D ((power OR voltage OR energy) ADJ2 (decreas* OR low OR dissipat* OR load OR reduc*)) 5D (constant ADJ1 gate ADJ1 depth) 5D ("AND" ADJ1 gate*) 5D (XOR OR (Exclusive ADJ1 "OR") OR EOR)) AND (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) AND (logarithmic ADJ1 delay)	61
19	18 AND G06F 7/483	5
20	18 AND G06F 7/506	0
21	18 AND G06F 7/507	0
22	18 AND G06F 7/575	1

Computer Accessed Text Databases Searched

The Patent Analyst searched the following computer accessed text databases:

Proquest: http://www.proquest.com/

#	Search query	Results
1	(linear 1W fast 1W adder)	1,517
2	author ("Juan Pablo Ramirez")	15
3	author ("Juan Pablo Ramirez") AND (linear 1W fast 1W adder)	0
4	author ("Juan Pablo Ramirez") AND ("Arithmetic Logic Unit" OR ALU)	0
5	author ("Juan Pablo Ramirez") AND ((Arithmetic 1W Logic 1W Unit) OR ALU)	0
6	((Arithmetic 1W Logic 1W Unit) OR ALU) AND (linear 1W fast 1W adder)	874
7	6 AND ((4 OR four) 1W bit 1W (adder OR register))	853
8	((1 OR one) 1W bit 1W (adder OR register))	7,221
9	((4 OR four) 1W bit 1W (adder)) AND ((1 OR one) 1W bit 1W (register))	1,018
10	((4 OR four) 1W bit 1W (adder)) AND ((1 OR one) 1W bit 1W (register)) AND (linear 1W fast 1W adder)	937
11	((4 OR four) 1W bit 1W (adder)) AND ((1 OR one) 1W bit 1W (register)) AND (linear 1W fast 1W adder) AND ((Arithmetic 1W Logic 1W Unit) OR ALU)	780
12	((4 OR four) 1W bit 1W (adder)) NEAR20 ((1 OR one) 1W bit 1W (register)) NEAR20 (linear 1W fast 1W adder) NEAR20 ((Arithmetic 1W Logic 1W Unit) OR ALU)	0
13	((4 OR four) 1W bit 1W (adder)) AND ((1 OR one) 1W bit 1W (register)) AND (linear 1W fast 1W adder) AND ((Arithmetic 1W Logic 1W Unit) OR ALU) AND (logarithmic 2W delay)	246
14	author ("Juan Pablo Ramirez") AND (linear NEAR4 adder)	0
15	author ("Juan Pablo Ramirez") AND (logarithmic NEAR4 delay)	0

PCT Application No.: PCT/US2023/066525
Date of Search: 23 August 2023

Google Scholar: https://scholar.google.com/

#	Search query	Results
1	(linear ADJ1 fast ADJ1 adder) AND ((Arithmetic ADJ1 Logic ADJ1 Unit) OR ALU)	100,000+
2	((Arithmetic 1 ADJ1 Logic ADJ1 Unit) OR ALU) AND (linear ADJ1 fast ADJ1 adder)	91,979
3	((Arithmetic 1 ADJ1 Logic ADJ1 Unit) OR ALU) AND (linear ADJ1 fast ADJ1 adder) AND ((1 OR one) ADJ1 bit ADJ1 (register))	52,870
4	((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND ((4 OR four) ADJ1 bit ADJ1 (adder*))	51,985
5	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND ((4 OR four) ADJ1 bit ADJ1 (adder*)	13,186
6	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND" ADJ1 gate*))	10,349
7	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND gate"))	2,561
8	(logarithmic ADJ1 delay) AND ((Arithmetic 1 ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("AND gate") NEAR20 (power ADJ1 dissipat*))	589
9	(logarithmic ADJ1 delay) AND ((Arithmetic ADJ1 Logic ADJ1 Unit*) OR ALU) AND (linear ADJ1 fast ADJ1 adder*) AND ((1 OR one) ADJ1 bit ADJ1 (register*)) AND (((4 OR four) ADJ1 bit ADJ1 (adder*)) NEAR20 ("XOR gate") NEAR20 (power ADJ1 dissipat*))	221
10	inventor:(Juan Pablo Ramirez)	157
11	(linear ADJ2 fast ADJ2 adder*)	100,000+
12	("4" OR four) ADJ1 bit ADJ1 adder*	100,000+
13	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 fast ADJ2 adder*) WITH (logarithmic ADJ1 delay)	23,241
14	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 fast ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (dissipat* OR load OR reduc*))	20,981
15	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR) WITH (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (low OR dissipat* OR load OR reduc*))	21,453
16	(("4" OR four) ADJ1 bit ADJ1 adder*) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR)	8,035

	WITH (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) WITH (logarithmic ADJ1 delay) WITH ((power OR voltage OR energy) ADJ2 (low OR dissipat* OR load OR reduc*)) WITH (constant ADJ1 gate ADJ1 depth)	
17	((("4" OR four) ADJ1 bit ADJ1 adder*) WITH ((power OR voltage OR energy) ADJ2 (decreas* OR low OR dissipat* OR load OR reduc*)) WITH (constant ADJ1 gate ADJ1 depth) WITH ("AND" ADJ1 gate*) WITH (XOR OR (Exclusive ADJ1 "OR") OR EOR)) AND (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) AND (logarithmic ADJ1 delay)	8,035
18	((("4" OR four) ADJ1 bit ADJ1 adder*) 5D ((power OR voltage OR energy) ADJ2 (decreas* OR low OR dissipat* OR load OR reduc*)) 5D (constant ADJ1 gate ADJ1 depth) 5D ("AND" ADJ1 gate*) 5D (XOR OR (Exclusive ADJ1 "OR") OR EOR)) AND (linear ADJ2 ((high ADJ1 speed) OR fast) ADJ2 adder*) AND (logarithmic ADJ1 delay)	323
19	18 AND G06F 7/483	12

Date search was completed: 23 August 2023

RB/AK