WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2023/066525

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-15	YES
	Claims	None	NO
Inventive step (IS)	Claims	1-15	YES
	Claims	None	NO
Industrial applicability (IA)	Claims	1-15	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-15 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest:

Regarding claim 1, the prior art of record, individually or in combination, does not teach or fairly suggest a linear fast adder for an Arithmetic Logic Unit (ALU), the adder comprising: a) a four-bit adder component comprising a plurality of logic gates comprising at least sixteen AND gates, four XOR gates; and b) a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Claims 2-15 depend from claim 1, and therefore meet the criteria set out in PCT Article 33(2)-(3) for at least the same reasons as claim 1.

The prior art teaches some of the concepts and/or aspects of the claim limitations as shown below, but does not teach the claim limitations in their entirety and as specifically recited in each of the claims, nor would it have been obvious to one of ordinary skill in the art to combine the prior art references to achieve the claim in its entirety:

Freeman (US 4,377,807 A) teaches a four-bit adder comprising two AND gates (see Fig. 3, col. 3, lines 35-65, four-bit adder 60, with AND gates 94 & 98). Freeman fails to teach a four-bit adder component comprising a plurality of logic gates comprising at least sixteen AND gates, four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Flahie (US 5,912,832 A) teaches a 4 x 4 bit fast multiplier comprising a plurality of AND gates (see Fig. 14, col. 7, lines 1-50, 4 x 4 bit fast multiplier CHA, with 16 AND gates 104). Flahie fails to teach a four-bit adder component comprising at least four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Nagendra teaches linear fast adder (see Pages 2-3, which teach that logic circuits designed for speed, such as a 32 bit adder, are faster and more complex, and general consume more area and power). Nagendra also teaches that (CMOS technology reduces power dissipation, see pages 7-9). Nagendra also teaches a variety of gate depth configurations (see pages 10-11).
Nagendra fails to teach a four-bit adder component comprising at least 16 AND gates; four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Dungavath teaches a variety of configurations of high-speed, low power consumption adders (see Dungavath, pages 2-4, 7, 12-13, 18 & 24-26). Dungavath fails to teach a four-bit adder component comprising at least 16 AND gates; four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Claims 1-15 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.